### 20.2.0 DIGITAL ELECTRONICS

### 20.2.01 Introduction

This unit deals with study of circuits of signals that take only two different levels. It is intended to provide the trainee with the relevant knowledge skills and attitudes necessary to make the learner competent in design, installation and maintenance of digital equipment and devices. The trainers may use phased design projects (suitable for the level) to enhance skills and competence acquisition.

## 20.2.02 General Objectives

At the end of the module unit, the trainee should be able to:

- a) Understand number systems and perform binary arithmetic
- b) Design combination logic networks
- c) Design flip-flop circuits
- d) Design Register and Counter Circuits
- e) Understand the operation of data handling logic circuits
- f) Apply arithmetic circuits in electronic circuits
- g) Appreciate digital electronics as a foundation for industrial controls

## 20.2.03 Module Unit Summary and Time Allocation

Digital Electronics

Digital Electronics					
Code	Sub Module Unit	Content	Time Hours		
20.2.1	Number systems	<ul> <li>Number systems</li> <li>Binary systems</li> <li>Conversion of numbers to binary and vice versa</li> <li>'Ones' and 'twos' complement s</li> <li>Arithmetic</li> <li>Numbers in octal</li> <li>Conversion of octal numbers into other numbers and vice versa</li> <li>Conversion of hexadecimal numbers to other number systems</li> <li>Application of number systems</li> </ul>	4		
20.2.2	Binary codes	<ul> <li>Importance of Binary codes</li> <li>BCD arithmetic</li> <li>BCD arithmetic</li> <li>Binary numbers in grey code</li> </ul>	6		

	1	41.1	
ļ		Alphanumeric codes	<u> </u>
		Application of alphanumeric	
		codes.	
	_	Error detection	
20.2.3	Logic gates	Operation of basic logic gates	6
	and Boolean	Operation of hybrid (derived)	
	algebra	logic gates	
		• The Boolean algebra	
		Reduction of logic expression	
		Implementation of logic circuits	
20.2.4	Combinationa	Definition of Combinational logic	6
	I logic design	network operation	
		Derivations from Boolean	
		Designing combinational logic	
		using Boolean algebra	
		Designing combinational circuits	
		using tabular methods	
		Logic circuits for industrial	
		interlock systems including time	
		delay	
20.2.5	Logic families	Transistor as a switch	4
		Classifications of Logic Families	
		Operation of various logic	
		families	
		• Handling requirements of various	
		logic Families	İ
		Interconnection of different logic	1
20.0.6	TOU O	families	0
20.2.6	Flip flops	• Latches	8
1		Types of flip-flops	
		Edge triggered	
		Master/slave flip-flop	
		Manufacturers data sheets and	
<u></u>		catalogues	
20.2.7	Combinationa	Definition of data handling logic	6
	1 logic circuits	circuits	
		Operation of data handling logic	}
	ļ	circuits	
		Applications	
	}	Similarities between decoder and	
<u></u>		demultiplexers	
20.2.8	Sequential	Shift register operation	8
1	logic circuits	Serial register operation	

Γ	<del></del>	<del></del>	
		Parallel register operation	
		Shift register modes	1
		Use of manufacturers data sheets	
1		and catalogues to identify	1
	]	registers	1
		Operation of ripple counters	
		Operation of synchronous	
		counters	
		Comparison between ripple and	
		synchronous	
İ		Feedback register	
		Application of counters	
	ľ	Use of manufacturers' data book	
		and catalogue to identify counters	
20.2.9	Arithmetic	Serial Adders	6
	Circuits	Parallel adder	
		Serial and parallel adder	
		Arithmetic circuits	
20.2.10	Converters	Operational amplifiers as	6
		Comparator C	
		Terminologies	
		Operation of DAC	
		Operation of ADC	İ
		Application	
20.2.11	Memories	Classification of memory devices	6
		Terminologies	_
		Operation of semiconductor RAM	
		and ROM memory devices	
		Organization of ROM memory	
		devices	
		Operation and organization of	
		secondary storage memories	
İ		Mapping	
		Memory organization	
Total '	Time		66
			<u>~~</u>

## 20.2.1 NUMBER SYSTEMS

### Theory

- 20.2.1T0 Specific objectives

  By the end of the submodule unit, the trainee should be able to:
  - represent numbers in decimal
  - b) represent numbers in binary
  - c) convert binary numbers into other number systems and vice versa
  - d) represent binary numbers into one's and two's complement
  - e) perform binary arithmetic
  - f) represent numbers in octal
  - g) convert octal numbers into other number systems and vice
  - h) represent numbers in hexadecimal
  - i) convert hexadecimal numbers to other number systems and vice versa
  - j) state the areas of application of number systems

#### Content

- 20.2.1T1 Number systems
- 20.2.1T2 Binary systems
- 20.2.1T3 Conversion of numbers to binary and vice versa
- 20.2.1T4 'Ones' and 'twos' complement s
- 20.2.1T5 Arithmetic
- 20.2.1T6 Numbers in octal

- 20.2.1T7 Conversion of octal numbers into other numbers and vice versa
- 20.2.1T8 Conversion of hexadecimal numbers to other number systems
- 20.2.1T9 Application of number systems

## 20.2.1C Competence

The trainee should have the ability to: number systems in programming

## 20.2.2 BINARY CODES

#### Theory

- 20.2.2T0 Specific objectives

  By the end of the submodule unit, the trainee should be able to:
  - a) explain the importance of various binary codes
  - b) represent decimal numbers in binary coded decimal (BCD)
  - c) perform BCD arithmetic
  - d) represent binary numbers in gray code
  - represent characters in various alphanumeric codes.
  - f) Identify the use of various alphanumeric codes in digital systems
  - g) explain various methods of error detection and correction

		Content			_	Identities and Rules,
20.2.2T	1	Importance of Binary				De Morgans
	-	codes				Theorems
20.2.2T	2	Representation of decimal	20.2.37	Г4	Mir	nimize logic
		numbers in Binary Coded				ressions using:
		Decimal (BCD)			-	Boolean algebra
20.2.2T	3	BCD arithmetic			-	K-Map upto 4
20.2.2T	4	Representation of binary				variables
		numbers in gray code	20.2.37	75	Imp	olement logic circuits
20.2.2T	5	Representation of			usii	ng
		characters in various			,	NAND gates only
		alphanumeric codes			ii)	NOR gates only.
20.2.2T	6	Use of alphanumeric				
		codes in digital systems			Pra	ictice
20.2.2T	7	Methods of error detection			_	
			20.2.3F			ecific Objectives
		OGIC GATES AND		-		end of the sub-
	BC	OOLEAN ALGEBRA				e unit the trainee
	-		~	<b>\</b>		be able to:
	Th	eory	-O)	a)		entify pin configuration
20.2.25	^	Constitution	$\mathcal{C}^{\circ}$	L)		logic gate ICs
20.2.3T		Specific objectives	·.	b)		ount the logic gate IC  a breadboard
		the end of the sub module		٥)		
		it, the trainee should be		c)		rify the operation of gic gates
		explain the operation of			108	gic gaies
	a)	the basic logic gate			C	mtent
	ы	explain the operation of	20.2.3F	)1		entifying pin
	υ,	hybrid (derived) logic	20.2.51	*		nfiguration
		gates	20.2.3F	2		ounting logic gate IC
	c)	understand the concepts	20.2.51	_		a breadboard
	٠,	of Boolean algebra	20.2.3F	3		emonstrate operation of
	d)	minimize logic		•		gic gates
	-,	expressions using				5 <b>6</b>
		universal gates	20.2.30	,	Co	mpetence
	e)	implement logic circuits				sinee should have the
	_,	using universal gates				to: construct and test
		5g			-	s logic gates
	Со	ntent				
20.2.3T		Basic Logic gates	Sugges	ted i	eac	hing/Learning
		AND, OR, INVERTER	Activiti			5
20.2.3T		Hybrid Gates	-	Illu	istra	etion
,,		NAND, NOR, Exclusive	-	De	mor	nstration
		gates	-			aking
20.2.3T3		Boolean algebra	-			al exercise

# Suggested Teaching and Learning Resources

- Digital trainer kit
- Assorted logic gate ICS
- Connecting wires
- Clock generator
- Breadboard
- DC power supply
- LED display

# Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

# 20.2.4 COMBINATIONAL LOGIC DESIGN

### Theory

- 20.2.4T0 Specific objectives

  By the end of the submodule unit, the trainee should be able to:
  - a) define combinational logic networks
  - design combinational logic circuits using Boolean algebra
  - c) design combinational logic circuits up to 4 input variables using Karnaugh map
  - d) design combinational logic circuits up to 4input variables using tabular method.
  - e) design combinational logic circuits for industrial interlock systems including time delay.

#### Content

- 20.2.4T1 Combination logic & Network design
- 20.2.4T2 Combinational logic circuits using Boolean algebra
- 20.2.4T3 Combinational logic circuits up to 4 input variables using Karnaugh map
- 20.2.4T4 Combinational logic circuits up to 4-input variables using tabular method
- 20.2.4T5 Combinational logic circuits for industrial interlock systems including time delay

#### **Practice**

- 20.2.4P0 Specific objectives

  By the end of the submodule unit, the trainee should be able to:
  - a) use manufacturers' data sheets and catalogues to identify characteristics and pin connections of ICs.
  - b) interconnected different logic families

#### Content

- 20.2.4P1 Use of manufacturer's data book
- 20.2.4P2 Interconnection of different logic families

### 20.2.4C Competences

The trainee should have the ability to: use different logics gates in electronic circuit design

# Suggested teaching/Learning Resources

- Logic gates
- Electronic tool kit
- Electrical measuring instruments
- Bread board

## Suggested teaching/Learning Activities

- Illustration
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

## Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

### 20.2.5 LOGIC FAMILIES

### Theory

- 20.2.5T0 Specific objectives

  By the end of the submodule unit, the trainee should be able to:
  - a) explain the use of a transistor as a switch
  - b) state classifications of logic families
  - explain the general operation and characteristics of various logic families
  - d) state the handling requirements for various logic families

#### Content

- 20.2.5T1 Transistor as a switch
  - i) BJT
  - ii) MOSFET
  - iii) Synchronous sequential logic
- 20.2.5T2 Classifications of Logic Families
  - i) BJT logic families
  - ii) MOSFET logic families
  - iii) SSI
  - iv) MSI
  - v) LSI
  - vi) VLSI
- 20.2.5T3 Operation of various logic families
- 20.2.5T4 Ccharacteristics of various logic families in terms of
  - i) Loading rules
  - ii) Wired AND operation
  - iii) Unused inputs
  - iv) Protection
  - v) Interfacing between logic families
  - vi) Tri-state TTLs
  - Use of manufacturers Datasheets
- Datasheets
  20.2.5T5 How to connect different
  - logic families
    i) TTL-CMOS
  - ii) MOS-TTL

### Practice

- 20.2.5P0 Specific Objectives

  By the end of the submodule unit, the trainee should be able to:
  - a) select a particular logic gate IC using data sheets or catalogs
  - b) demonstrate the operation of logic gates
     ICs

- e) interface different logic gates
- d) interconnect various logic families

#### Content

- 20.2.5P1 Selecting a particular logic gate IC from a catalogue
- 20.2.5P2 Demonstrating the operation of logic gate ICS
- 20.2.5P3 Interfacing different logic gates

### 20.2.5C Competence

The trainee should have the ability to: construct and test logic circuits from different logic families

# Suggested teaching/Learning Activities

- Illustration
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

# Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

### 20.2.6 FLIP-FLOPS

### Theory

- 20.2.6T0 Specific objectives

  By the end of the sub module unit, the trainee should be able to:
  - a) explain the operation of latches

- b) explain the operation of various flip-flop circuits.
- c) explain the operation of edge triggered flip-flops
- d) explain characteristics of master/slave flip-flops
- e) use manufacturers' data sheets and catalogues to select flip-flops.

### Content

- 20.2.6T1 Explanation of operation of latches
  - i) Transistor latch
  - ii) NAND latch
  - iii) NOR latch
  - iv) 20.2.6T2Flip-flops
  - v) S-R
  - vi) J-K
  - vii) D Type
  - viii) T-type
- 20.2.6T3 Explanation operation of the following using transition tables and
  - i) wave forms:
  - ii) Edge triggered
  - iii) Master/slave flip-flop
- 20.2.6T4 Characteristics of master/slave flip flops
- 20.2.6T5 Use manufacturers data sheets and catalogues to identify:
  - i) Pin connection
  - ii) Characteristics of IC flip-flops

#### **Practice**

- 20.2.6P0 Specific Objectives

  By the end of the submodule unit, the trainee should be able to:
  - a) select a particular flip flop IC using data sheets or catalogs

b) demonstrate the operation of various flip flops

#### Content

20.2.6P1 Selecting a particular flip flop IC for using data sheets or catalogues

20.2.6P2 Demonstrating the operation of various flip flops

## 20.2.6C Competence

The trainee should have the ability to: construct and test logic circuits from different flip flops.

# Suggested teaching/Learning Activities

- Illustration
- Demonstration
- Note taking
- Observation
- Practical exercise

## Suggested teaching/Learning Resources

- Logic circuits
- Flip flops
- Electrical measuring instruments

# Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

# 20.2.7 COMBINATION LOGIC DESIGN

## Theory

20.2.7T0 Specific objectives

By the end of the submodule unit, the trainee should be able to:

- a) define data handling combinational logic circuits
- b) explain the operation of combinational logic circuits
- c) describe applications combinational logic circuits
- d) state similarities between decoder and demultiplexers

#### Content

20.2.7T1 Definition of combinational logic circuits

- i) Decoders
- ii) Encoders
- iii) Multiplexers
- iv) Demultiplexers
- 20.2.7T2 Explanation of the operation of combinational logic circuits
  - i) Decoders
  - ii) Encoders
  - iii) Multiplexers
  - iv) Demultiplexers
- 20.2.7T3 Application of
  - i) Decoders
  - ii) Encoders
- 20.2.7T4 Similarities of Multiplexers and Demultiplexers

#### **Practice**

- 20.2.7P0 Specific Objectives

  By the end of the sub 
  module unit, the trainee
  should be able to:
  - a) construct various
     combinational logic
     circuits
  - b) demonstrate the operation of various combinational logic circuits

#### Content

- 20.2.7P1 Constructing various combinational logic circuits
- 20.2.7P2 Demonstrating operation of various combinational logic circuits

## 20.2.7C Competence

The trainee should have the ability to: construct and test various combinational logic circuits.

# Suggested teaching/Learning Activities

- Discussion
- Ouestion and answer
- Demonstration
- Note taking
- Observation
- Practical exercise

# Suggested teaching/Learning Resources

- i) Electrical measuring instruments
- ii) Electronic tool kit
- iii) Dc Power supply
- iv) Ac power supply
- v) Logic gates
- vi) Electronic components

# Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

# 20.2.8 SEQUENTIAL LOGIC CIRCUITS

#### Theory

- 20.2.8T0 Specific objectives
  By the end of the submodule unit, the trainee
  should be able to:
  - explain the basic operation of a shift register
  - describe serial shift register operation
  - describe parallel shift register operation
  - d) explain the practical IC shift modes of operation
  - use manufacturers data sheets and catalogues to identify ICs
  - f) describe the operation of asynchronous (ripple through) counters
  - g) describe the operation of synchronous counters
  - compare synchronous with asynchronous counters
  - i) describe operation of feedback register
  - j) describe the applications of counters
  - k) use manufacturer's data sheets and catalogues to identify and select counters.

		Content	20.2.8
20	.2.8T1	Operation of a shift	
		register using	
		i) Transition tables	
		ii) Waveforms	
20	.2.8T2	Describe serial shift	
		register operation	
		i) Shift right	
		ii) Shift left	20.2.8
		iii) Shift around	
20	.2.8T3	Describe parallel shift	
		operation	
20	.2.8T4	Explain the practical IC	
		shift register modes	
		i) SISO	
		ii) SIPO	
		iii) PIPO	
		iv) PISO	
20	.2.8T5	Use manufacturers data	20.2.8
		sheets and catalogues to	~
		identify	20.2.8
		i) Pin connection	x .0
		ii) Characteristics of IC	100
		flip-flop	20.2.8
20.	.2.8T6	Describe the operation of	7
		the Ripple counter	
		i) Modulus number	
		ii) Stage and state	
		numbers	
		iii) Shortened mod	Sugges
		iv) Decoding outputs	Activit
		v) Waveforms	-
		vi) Limitations	-
20.	2.8T7	Describe the operation of	-
		synchronous counters	-
20.	2.8T8	Compare asynchronous	_
		and synchronous counter	-
20.	2.8T9	Describe the operation of	-
		the feedback register	
		i) Ring counter	Sugges
		ii) Twisted ring counter	Resour
		iii) Random sequence	-
		generator	

20.2.8T10 Describe applications of

counters

20.2.8T11 Use manufacturer's data sheets and catalogues to identify:

- i) Pin connection
- ii) IC characteristics

#### **Practice**

20.2.8P0 Specific Objectives

By the end of the submodule unit the trainee should be able to:

- a) construct various sequential logic circuits
- b) operate various sequential logic circuits

#### Content

20.2.8P1 Constructing various sequential logic circuits
20.2.8P2 Operation of various sequential logic circuits

# 20.2.8C Competence

The trainee should have the ability to: construct and test various sequential logic circuits

# Suggested teaching/Learning Activities

- Discussion
- Question and answer
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

# Suggested teaching/Learning Resources

- Electrical measuring instruments
- Electronic tool kit
- Dc Power supply
- Sequential logic circuits

- Electronic components
- Assorted cables and other electrical materials

# Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

### 20.2.9 ARITHMETIC CIRCUITS

- 20.2.9T0 Specific Objectives

  By the end of the submodule unit, the trainee
  should be able to:
  - a) describe the operation of a serial adder
  - b) describe the operation of a parallel adder
  - c) compare serial and parallel adders
  - d) describe the application of arithmetic circuits

#### Content

- 20.2.9T1 Description of operation of serial adders
  - i) Operation
  - ii) Modification to perform subtraction
  - iii) Limitation
- 20.2.9T2 Description of parallel adder
  - i) Operation
  - ii) Use and operation of a look-ahead carry
- 20.2.9T3 Explanation of comparison of serial and parallel adders
  - i) Operation
  - ii) Complexity

# 20.2.9T4 Description of arithmetic circuits

 Applications of adders e.g. ALU

#### **Practice**

- 20.2.9P0 Specific Objectives

  By the end of the sub module unit the trainee should be able to:
  - a) construct various arithmetic circuits
  - b) demonstrate the operation of various arithmetic circuits

#### Content

- 20.2.9P1 Constructing various arithmetic circuits
- 20.2.9P2 Demonstrating operation of various arithmetic circuits

## 20.2.9C Competence

The trainee should have the ability to: construct and test various arithmetic circuits.

# Suggested teaching/Learning Activities

- Discussion
- Ouestion and answer
- Illustration
- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

# Suggested teaching/Learning Resources

- Electrical measuring instruments
- Electronic tool kit
- Electrical tool kit

- Dc Power supply
- Ac power supply
- Three phase power supply
- Arithmetic circuits
- Electronic components
- Assorted cables and other electrical materials

## Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project
- Project Report writing and presentation

### 20.2.10 CONVERTERS

## Theory

- 20.2.10T0 Specific Objectives
  By the end of the submodule unit, the trainee
  should be able to:
  - a) describe Operational Amplifier as comparator
  - b) define the terminologies used in converter circuits
  - c) describe the operation of DAC
  - d) describe the operation of ADC
  - e) explain the applications of converter circuits

#### Content

- 20.2.10T1 Operational Amplifier as Comparator
- 20.2.10T2 Definition of DAC's and ADC's terminologies
- 20.2.10T3 Digital to Analogue Converter
  - i) Types
  - ii) Analysis
  - iii) Application

- 20.2.10T4 Analogue to Digital Converter
  - i) Types
  - ii) Analysis
- 20.2.10T5 Applications

#### **Practice**

- 20.2.10P0 Specific Objectives

  By the end of the submodule unit the trainee should be able to:
  - a) construct various converter circuits
  - b) demonstrate operation of various converter circuits

#### Content

- 20.2.10P1 Constructing various converter circuits 20.2.10P2 Operation of various
- 20.2.10P2 Operation of variou converter circuits

## 20.2.10C Competence

The trainee should have the ability to: construct and test various converter circuits.

# Suggested teaching/Learning Activities

- Demonstration
- Note taking
- Observation
- Practical exercise
- Project work

# Suggested teaching/Learning Resources

- i) Electrical measuring instruments
- ii) Electronic tool kit
- iii) Dc Power supply
- iv) Signal generators
- v) Electronic devices
- vi) Electronic components

# vii) Assorted cables and other

# Suggested Evaluation Methods

- Oral tests
- Timed written tests
- Assignments
- Timed practical tests
- Project

## **20.2.11 MEMORIES**

## Theory

- 20.2.11TO Specific Objectives

  By the end of the sub module unit, the trainee should be able to:
  - a) classify memories into various categories
  - b) define memory terminologies
  - c) describe the operations of semiconductor RAM and ROM memories
  - d) describe the organization of semiconductor ram and ROM
  - e) describe the operation and organization of secondary storage memories
  - f) explain memory map
  - g) describe memory organization

#### Content

- 20.2.11T1 Classification of Memories into various categories in a computer system
- 20.2.11T2 Stating the meaning of various memory terminologies

- 20.2.11T3 Description of operation of Semiconductor RAM and ROM
  - i) Memory cell
  - ii) Dynamic & Static memories
  - iii) Erasable and nonerasable memories
  - iv) Access timing of memories
  - v) Memory capacity
- 20.2.11T4 Description of organization of Semiconductor RAM and ROM
  - Register representation in memories
  - ii) Memory timing
  - iii) Memory expansion
  - iv) Memory address decoding
  - v) Memory pages
  - vi) Cache memories
  - vii) Storage capacity
- 20.2.11T5 Description of organization and operation of Secondary storage devices
  - i) Need for secondary storage
  - ii) Magnetic bubble memories
  - iii) Floppy & hard disks
  - iv) Recording surfaces
  - v) Accessing & timing
  - vi) Formats
  - vii) Disk drives
  - viii) Storage capacity
  - ix) Hard disk
  - x) CD ROM
  - xi) CCD
  - xii) Data stick/Flash Disc
- 20.2.11T6 Description of memory mapping

- i) Address decoders
- ii) Address allocation
- iii) System ROM, RAM, I/O, Expansion
- iv) Expansion slots
- v) Timing
- vi) Pages
- 20.2.11T7 Description of memory organization
  - i) Hierarchy
  - ii) Timing
  - iii) Formats
  - iv) Capacity
  - v) Functions
- 20.2.11C Competence
  Ability to manage
  computer memories